

The following listing of claims will replace all prior versions, and listings, of claims in the application, in which deleted matter is shown using ~~striketrough~~ and added matter is underlined:

**Listing of Claims:**

1. (Original) A controller for regulating a FET to operate as a pass device, the FET including a gate and a current path having an input and an output, said controller comprising:  
  
input, output and gate nodes for coupling to the current path input, the current path output and the gate of the FET, respectively;  
  
a voltage source, coupled to said input node, that provides a regulation voltage level relative to the input node;  
  
a controlled low current device, coupled to said gate node and having a control input; and  
  
a high gain regulation amplifier having a first input coupled to said output node, a second input coupled to said voltage source, and an output coupled to said control input of said controlled low current device to regulate the FET;  
  
wherein said regulation amplifier functions as a small signal oscillator.
2. (Original) The controller of claim 1, wherein said regulation amplifier oscillates while regulating a voltage difference between said input and output nodes to said regulation voltage level and wherein said controlled low current device presents a high impedance to said gate node to prevent oscillations from disturbing regulation operation.
3. (Original) The controller of claim 1, wherein said controlled low current device comprises:  
  
a weak current source providing a low level current to said gate node; and

a weak current sink device that draws a low level current from said gate node based on said control input;

wherein said regulation amplifier controls said weak current sink device to contradict said weak current source to maintain regulation.

4. (Original) The controller of claim 1, further comprising:

a current sink device, coupled to said gate node and having a control input, that sinks current from said gate node when activated sufficient to turn off the FET within a first predetermined amount of time; and

a first delay filter circuit coupled between said output of said regulation amplifier and said control input of said current sink device;

wherein said first delay filter circuit activates said current sink device if said regulation amplifier goes out of regulation in one direction for a first predetermined delay that is sufficiently less than said first predetermined amount of time.

5. (Original) The controller of claim 4, wherein said first delay filter circuit comprises:

an amplifier circuit that compares said output of said regulation amplifier with a regulation voltage level and that asserts a disable signal indicative thereof; and

a delay filter, coupled to said current sink device and that receives said disable signal.

6. (Original) The controller of claim 4, further comprising:

a current source device, coupled to said gate node and having a control input, that sources current to said gate node when activated sufficient to turn on the FET within a second predetermined amount of time; and

a second delay filter circuit coupled between said output of said regulation amplifier and said control input of said current source device;

wherein said second delay filter circuit activates said current source device if said regulation amplifier goes out of regulation in an opposite direction for a second predetermined delay that is sufficiently less than said second predetermined amount of time.

7. (Original) The controller of claim 6, wherein said second delay filter circuit comprises:

an amplifier circuit that compares said output of said regulation amplifier with a regulation voltage level and that asserts a regulation signal indicative thereof; and

a delay filter, coupled to said current source device and that receives said regulation signal.

8. (Original) The controller of claim 1, further comprising a high speed comparator circuit having inputs coupled to said input and output nodes and an output coupled to said gate node for turning off the FET when a voltage of said input node drops below a voltage of said output node by a threshold voltage level.

9. (Original) The controller of claim 8, wherein said high speed comparator circuit comprises:

a compensation circuit, coupled to said output node, providing said threshold voltage level;

a current sink device, coupled to said gate node and having a control input, that sinks a high current from said gate node when activated sufficient to turn off the FET within a predetermined amount of time; and

a comparator having a first input coupled to said input node, a second input coupled to said compensation circuit, and an output coupled to said control input of said current sink device.

10. (Original) The controller of claim 1, further comprising a floating voltage source providing a voltage reference node relative to said input node for providing power to circuitry coupled between said input and voltage reference nodes.

11. (Currently amended) The controller of claim 10, wherein said controlled low current source device comprises:

a weak current device, coupled to said voltage reference node, having said control input and an output; and

a current gain mirror, coupled between said input and gate nodes and having a control input coupled to said control input of said weak current device, and operative to sink a proportionate current from said gate node to said input node generated by said weak current device.

12. (Original) A pass device for coupling an output of a power converter to a power bus, comprising:

a FET having a gate, an input for coupling to the power converter output and an output for coupling to the power bus; and

a FET controller, comprising:

a high gain regulator, having first and second inputs and an output coupled to said input, said output and said gate of said FET, respectively, that regulates a voltage difference between said input and output of said FET to a regulation voltage level; and

a high speed comparator circuit, having first and second inputs coupled to said input and output of said FET and an output coupled to said gate of said FET, that quickly turns off said FET if the said voltage difference reaches a predetermined threshold voltage level indicative of a fault with the power converter;

wherein said regulator operates as a small signal oscillator.

13. (Original) The pass device of claim 12, wherein said FET controller further comprises a delayed filter current sink, coupled between said gate of said FET and said output of said regulator, that turns off said FET if said regulator surpasses a predetermined level for a predetermined time period.
14. (Original) The pass device of claim 13, wherein said delayed filter current sink comprises:

a current sink coupled to said gate of said FET and having a control input; and

a delay filter coupled between said output of said regulator and said control input of said current sink.
15. (Original) The pass device of claim 12, wherein said FET controller further comprises a delayed filter current source, coupled between said gate of said FET and said output of said regulator, that turns on said FET if said regulator surpasses a predetermined level for a predetermined time period.
16. (Original) The pass device of claim 15, wherein said delayed filter current source comprises:

a current source coupled to said gate of said FET and having a control input; and

a delay filter coupled between said output of said regulator and said control input of said current source.
17. (Original) The pass device of claim 12, wherein said regulator comprises:

a voltage source coupled to said input of said FET and providing said regulation voltage level relative to said input of said FET;

a high gain amplifier having a first input coupled to said voltage source, a second input coupled to said output of said FET, and an output; and

a current device having an output coupled to said gate of said FET and a control input coupled to said output of said high gain amplifier.

18. (Original) The pass device of claim 17, wherein said high gain amplifier oscillates said current device during regulation and wherein said current device presents a relatively high impedance to said gate of said FET.

19. (Original) The pass device of claim 17, wherein said current device comprises:

a current source that sources current to said gate of said FET; and

a controlled current sink having a control input coupled to said output of said high gain amplifier;

wherein said high gain amplifier controls said controlled current sink to counterbalance said current source during regulation.

20. (Original) The pass device of claim 12, wherein said high speed comparator circuit comprises:

a compensation circuit coupled to said output of said FET that provides said threshold voltage level relative to said output of said FET;

a comparator having a first input coupled to said input of said FET, a second input coupled to said compensation circuit and an output; and

a high level current sink having an output coupled to said gate of said FET and a control input coupled to said output of said comparator.

21. (Original) An integrated circuit (IC) that implements a FET controller for controlling a FET to operate as a pass device between a power supply and a power bus in a redundant power system, said IC comprising:
- input, output and gate pins for coupling to an output of the power supply, an input of the power bus and a gate of the FET, respectively;
- an oscillating regulator having first and second inputs and an output coupled to said input, output and gate pins, respectively, that provides a high impedance regulation current to said gate pin;
- a delay filter current device, having a control input coupled to said output of said regulator and an output coupled to said gate pin, that sources current to said gate pin to slowly turn on the FET if said regulator rails in one direction for a first predetermined time period and that sinks current from said gate pin to slowly turn off the FET if said regulator rails in an opposite direction for a second predetermined time period; and
- a high speed comparator having first and second inputs and an output coupled to said input, output and gate pins, respectively, that draws a high current from said gate pin to quickly turn off the FET if said input pin falls below said output pin by a threshold voltage.